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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/799,479	03/12/2004	Kenneth Hubbard	CIS03-68(8178)	8394

47654 7590 03/01/2007

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EXAMINER	
KUNZER, BRIAN	
ART UNIT	PAPER NUMBER
2814	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/01/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/799,479	HUBBARD ET AL.	
	Examiner	Art Unit	
	Brian Kunzer	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) (amendment) filed on *27 November 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 13,15-18,20, and 29-33 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 13,15-18,20, and 29-33 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Amendments

Applicant's amendments, filed November 27th, 2006 has been received and entered. In summary, claims 1-12, 14, 19, and 21-28 have been cancelled and new claims 30-33 have been added, thus claims 13, 15-18, 20, and 29-33 are now pending examination.

Claim Objections

Claim 33 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. All of the limitations of claim 33 are previously provided for in claim 13.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 13, 15, 18, 20, and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jackson (US Patent No. 6,627,822) in view of Byun (US Patent No. 6,736,306) and further in view of Kalidas (US Patent No. 6,396,136).

With respect to claim 13, Jackson teaches, from figs. 1A-1D and 5, the method for manufacturing an area array package comprising:

coupling a grid array of primary electrical contacts (120) to a coupling surface of a substrate (108) within a central portion defined by the substrate, the grid array of primary electrical contacts (120) configured to carry at least data signals between the area array package (108) and a circuit board (101) (see column 4, lines 6-12);

forming the primary electrical contacts as a plurality of solder balls (114), each primary solder ball of the grid array defining a first diameter;

coupling a series of secondary electrical contacts (110) to the coupling surface of the substrate (108) within a peripheral area defined by the coupling surface, the series of secondary electrical contacts configured to carry power signals between the area array package (108) and the circuit board (101) (see column 4, lines 2-6), the series of secondary electrical contacts (110) separate from the grid array;

wherein coupling the series of secondary electrical contacts (110) comprises coupling the series of secondary electrical contacts (110) to the coupling surface of the substrate (108), the coupling surface configured to oppose a mounting surface of the circuit board (101).

However, Jackson does not teach forming the series of secondary electrical contacts as a plurality of secondary solder balls, each secondary solder ball of the series defining a second diameter, the second diameter defined by each of the secondary solder balls being greater than the first diameter defined by each of the primary solder balls. Instead, Jackson teaches the use of pins as the secondary electrical contacts.

Byun, drawn to ball grid array design for flip chips, does teach, from figs. 5 and 6, forming the series of secondary electrical contacts as a plurality of secondary solder balls (162), each secondary solder ball of the series defining a second diameter, the second diameter defined by each of the secondary solder balls being greater than the first diameter defined by each of the primary solder balls (160).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to create the device of Jackson utilizing the ball grid array of Byun as this would simply replace the pins of Jackson with larger diameter solder balls which still has the same desired effect as described by Jackson to create,

> "an electronic assembly for making power and signal connections between two substrates or between a semiconductor chip, socket or other device and a circuit board or the like that separates the power and signal connections, utilizes the appropriate type of connection and size and shape connection for the function being performed, makes efficient use of available area for making power and signal connections by minimizing the area on the chip or die and on the circuit board needed for making power and signal connections, and may be made efficiently with compatible manufacturing techniques or processes to form both the power and signal connections." (column 2, lines 2-13)

Additionally, the following limitations are not described in detail by Byun et al. or Jackson et al., yet the Examiner contends that the following constitutes a standard method of routing power and ground connections in a chip (die) attachment such as a printed circuit or mother board and as such, would be an obvious inclusion for the devices of Byun and Jackson. Nevertheless, Kalidas et al. does teach from fig. 7 and column 7, line 54 – column 8, line 15:

the substrate (703) having at least one power plane (703a), at least one ground plane (703b), at least one plated through hole (outer through holes) in communication with the at least

one power plane, and at least one plated through hole (inner through holes) in communication with the ground plane;

the substrate having a contact pad in electrical communication with the at least one plated through hole (outer through holes) in communication with the at least one power plane (703a) and electrically coupled with a secondary solder ball of the series of secondary electrical contacts;

the substrate having a contact pad in electrical communication with the at least one plated through hole (inner through holes) in communication with the at least one ground plane (703b) and electrically coupled with a secondary solder ball of the series of secondary electrical contacts;

the secondary solder ball, contact pad, and the at least one plated through hole (outer through holes) in communication with the at least one power plane (703a) configured to carry power to the at least one power plane through the coupling surface; and

the secondary solder ball, contact pad, and the at least one plated through hole (inner through holes) in communication with the at least one ground plane (703b) configured to carry power from the at least one ground plane through the coupling surface."

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to have the combined device of Jackson and Byun feature the power and ground routing substrate of Kalidas in order to increase flexibility and compatibility by providing a standardized routing solution. (See column 8, lines 10-15.)

With respect to claim 15, Jackson, from fig. 5, and Byun, from fig. 8c, teaches the method wherein the step of forming the series of secondary electrical contacts (pins of Jackson or second set of solder balls of Byun) comprises:

placing at least two solder balls on a contact pad oriented within the peripheral area defined by the coupling surface, each solder ball defining a first diameter,

heating the at least two solder balls to cause the solder to undergo reflow (see column 5, lines 16-18 of Byun)

forming a secondary solder ball on the contact pad, secondary solder ball of the [series] defining a second diameter, the second diameter defined by the secondary solder ball being greater than the first diameter defined by each of the primary solder balls.

With respect to claim 18, Jackson, combined with Byun and Kalidas, discloses all the limitations except for specifically teaching the method wherein the substrate defines a length of at least approximately 60 mm and a width of at least approximately 60 mm. It would have been obvious to have a substrate with the dimensions of 60mm X 60mm, since such a modification would have involved a mere change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art. In re Rose, 105 USPQ 237 (CCPA 1955).

Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC

Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669,149 USPQ 47 (CCPA 1966). Note also that it has been held that to be entitled to weight in method claims, the recited-structure limitations therein must affect the method in a manipulative sense, and not to amount to the mere claiming of a use of a particular structure. Ex parte Pfeiffer, 1962 C.D. 408 (1961).

With respect to claim 20, Jackson, combined with Byun and Kalidas, discloses all the limitations except for specifically teaching the method wherein the grid array of primary solder balls is configured in an array pattern of 50 columns having 50 primary solder balls per column. It would have been obvious to have a 50 X 50 grid array, since such a modification would have involved a mere change in the size of a component wherein the number of solder balls could easily be changed with a change in solder ball diameter or substrate area. A change in size is generally recognized as being within the level of ordinary skill in the art. In re Rose, 105 USPQ 237 (CCPA 1955).

Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669,149 USPQ 47 (CCPA 1966). Note also that it has been held that to be entitled to weight in method claims, the recited-structure limitations therein

must affect the method in a manipulative sense, and not to amount to the mere claiming of a use of a particular structure. Ex parte Pfeiffer, 1962 C.D. 408 (1961).

With respect to claim 29, Jackson teaches, from figs. 1A-1D and 5, the method further comprising surface mounting a die (chip) to a second surface of the substrate (socket), the second surface of the substrate (socket) opposing the coupling surface of the substrate, to inherently electrically couple the die (chip) with the first set of contact pads and the second set of contact pads (see column 2, lines 64-67) wherein the die is configured to exchange, through second surface of the substrate, at least data signals with the circuit board (of Kalidas) through the grid array of primary electrical contacts (114) and wherein the die is configured to exchange, through second surface of the substrate, power signals with the circuit board (of Kalidas) via the at least one secondary solder ball (Jackson's pins (110) replaced by Byun solder balls), the at least one contact pad, and the at least one plated through hole (of Kalidas).

With respect to claim 30, Jackson teaches, from figs. 1A-1D and 5, the method further comprising:

the grid array of primary electrical contacts (120) configured to carry data signals between the area array package (108) and a circuit board (101); coupling the series of secondary electrical contacts (110) to the coupling surface of the substrate (101) comprises coupling the series of secondary electrical contacts to the coupling surface of the substrate within the peripheral area defined by the coupling surface, the series of secondary electrical contacts (110) configured to carry power signals between the area array package and the circuit board.

Jackson, combined with Byun and Kalidas, does not specifically teach the method wherein the substrate has a length that is greater than 45 mm and has a width that is greater than 45 mm, nor that the primary electrical contacts couple to surface of the substrate in an array pattern of 50 columns having 50 primary electrical contacts per column within the central portion defined by the substrate, nor that a sum of the primary electrical contacts and the secondary electrical contacts being greater than 2500 electrical contacts.

Regardless, it would have been obvious to have a substrate with the dimensions of 60mm X 60mm, having an array pattern of 50 columns having 50 primary electrical contacts per column, and having a sum of the primary electrical contacts and the secondary electrical contacts being greater than 2500 electrical contacts, since such a modification would have involved a mere change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art. In re Rose, 105 USPQ 237 (CCPA 1955).

Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669,149 USPQ 47 (CCPA 1966). Note also that it has been held that to be entitled to weight in method claims, the recited-structure limitations therein must affect the method in a manipulative sense, and not to amount to the mere claiming of a use of a particular structure. Ex parte Pfeiffer, 1962 C.D. 408 (1961).

With respect to claim 31, Jackson teaches, from figs. 1A-1D and 5, the method wherein coupling the grid array of primary electrical contacts (120) to the coupling surface of the substrate within the central portion defined by the substrate, the grid array of primary electrical contacts configured to carry at least data signals between the area array package (108) and the circuit board (101) comprises coupling the grid array of primary electrical contacts to the coupling surface of the substrate within the central portion defined by the substrate, the grid array of primary electrical contacts configured to carry data signals and power signals between the area array package and the circuit board.

With respect to claim 32, Jackson, combined with Byun and Kalidas, discloses all the limitations except for specifically teaching the method wherein the substrate defines a length of at least approximately 60 mm and a width of at least approximately 60 mm. It would have been obvious to have a substrate with the dimensions of 60mm X 60mm, since such a modification would have involved a mere change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art. In re Rose, 105 USPQ 237 (CCPA 1955).

Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669,149 USPQ 47 (CCPA 1966). Note also that it has

been held that to be entitled to weight in method claims, the recited-structure limitations therein must affect the method in a manipulative sense, and not to amount to the mere claiming of a use of a particular structure. Ex parte Pfeiffer, 1962 C.D. 408 (1961).

With respect to claim 33, Kalidas teaches from fig. 7 and column 7, line 54 – column 8, line 15, the method comprising:

forming the substrate (703) having at least one power plane (703a) and at least one ground plane (703b);

forming plated through holes in the substrate such that at least one plated through-hole is in communication with the at least one power plane (703a) and at least one plated through hole in communication with the ground plane (703b), the plated through holes being disposed about the peripheral area defined by the coupling surface; and

coupling the series of secondary electrical contacts to the coupling surface of the substrate within the peripheral area defined by the coupling surface comprises coupling the secondary electrical contacts to the coupling surface of the substrate such that the secondary electrical contacts are in electrical communication with the plated through holes formed in the substrate and such that the secondary electrical contacts are disposed within the peripheral area defined by the coupling surface.

2. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jackson (US Patent No. 6,627,822), Byun (US Patent No. 6,736,306), and Kalidas (US Patent No. 6,396,136) as applied to claim 13 above, and further in view of Barber (US Patent No. 6,600,220).

With respect to claim 16, Jackson and Byun teach the method described above.

Jackson and Byun do not specifically teach the coupling of at least one power regulation device to the substrate and in electrical communication with the series of secondary electrical contacts.

Barber, drawn to power distribution in multi-chip modules, teaches, from fig. 1A, coupling a plurality of voltage converters (42) (i.e. a power regulation device) to a substrate (28) in communication with the power supply lines (34) (i.e. series of secondary electrical contacts).

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to create the device of Jackson coupled with the power regulation scheme of Barber permitting "the multi-chip module (MCM) to receive power at higher voltages than is supported by the high-density thin-film circuit region, decreasing MCM input current magnitudes and reducing noise and energy losses." (abstract of 6,600,220)

3. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jackson (US Patent No. 6,627,822), Byun (US Patent No. 6,736,306), and Kalidas (US Patent No. 6,396,136) as applied to claim 13 above, and further in view of Amir (US Patent No. 6,787,920).

With respect to claim 17, Jackson, combined with Byun, discloses all the limitations except for specifically teaching that the method comprises coupling the plurality of secondary solder balls to the substrate at a pitch of at least approximately 5 mm.

However integrated circuit (IC) package designers take into account several design parameters when deciding on the dimension for the pitch (i.e. the interval spacing of the contacts), including the well-known problem of bridging. Bridging occurs during the solder reflow process in which two separate contacts will merge together and short out the circuit because there is a too fine of a pitch. (See column 1, line 66 – column 2, line 8 of Amir.)

Therefore, it would have been obvious to one of ordinary skill in the art, at the time of invention, to have the combined device of Jackson, Byun, and Kalidas and have the appropriately sized pitch, such as 5mm, in order to reduce the bridging effect as disclosed by Amir because this specific dimension is the result of finding an optimized parameter for a well known problem which is typically accounted for in all similar devices; and a change in size and discovering an optimum value of a result effective variable is generally recognized as being within the level of ordinary skill in the art. In re Rose, 105 USPQ 237 (CCPA 1955). In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Response to Arguments

4. Applicant's arguments filed on November 27th, 2006 with respect to claims 13, 15-18, 20, and 29 have been considered but are moot in view of the new ground(s) of rejection (where Kalidas has been used).

The rejection of claims 13, 15-18, 20, and 29 under 35 U.S.C. 101 and 35 U.S.C. 112 2nd paragraph has been withdrawn.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian Kunzer whose telephone number is (571) 272-5054. The examiner can normally be reached on Monday-Friday 8:00-4:30 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BK
2/16/2007

ANH D. MAI
PRIMARY EXAMINER